P U C E N G E N H A R I A

PONTIFÍCIA UNIVERSIDADE CATÓLICA

CURSO DE ENGENHARIA ELÉTRICA

LABORATÓRIO DE SISTEMAS DIGITAIS 2 – SD 2

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Versão: 1. 2016

ÍNDICE:

EXPERIÊNCIA **1**

BIESTÁVEIS

Identificação dos alunos:	**Data:**
1.	**Turma:**
2.	
3.	**Professor:**
4.	
5.	**Conceito:**

I. OBJETIVOS:

- Implementação de Circuitos Biestáveis.

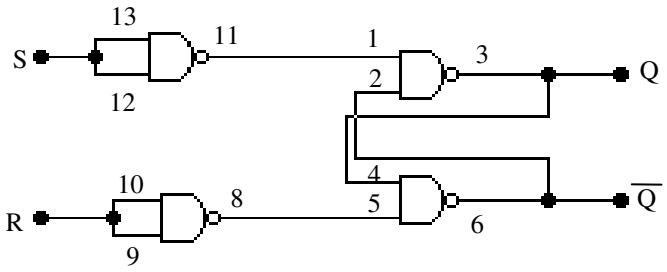
II. MATERIAL UTILIZADO:

- Placa Didática.
- Fonte CC de 5 V.
- CIs: 7400 (1), 7476 (1).

III. PROCEDIMENTO EXPERIMENTAL:

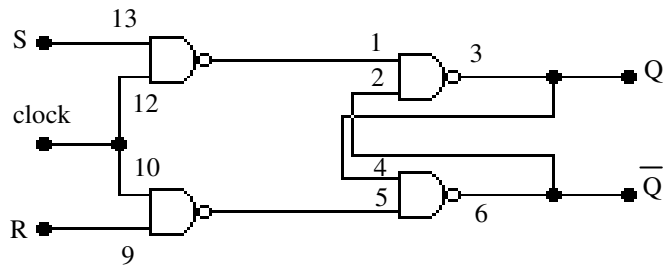
a) Monte um biestável tipo SC (Set/Clear) também conhecido por RS (Reset/Set) assíncrono utilizando apenas portas NAND e preencha a tabela verdade.

S	**C(R)**	**Q**	$\overline{Q}$	**Status**
0	**0**			
0	**1**			
1	**0**			
1	**1**			



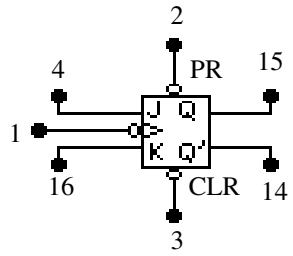
b) Monte um biestável tipo SC (RS) síncrono sensível a nível alto, utilizando apenas portas NAND, e preencha a tabela verdade.

CK	**S**	**C(R)**	**Q**	$\overline{Q}$	**Status**
⎍	**0**	**0**			
⎍	**0**	**1**			
⎍	**1**	**0**			
⎍	**1**	**1**			



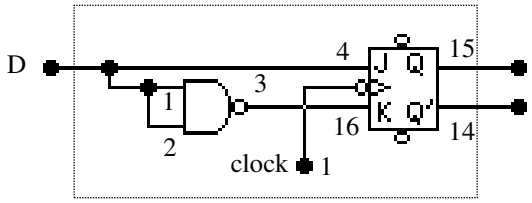
c) Verifique o funcionamento do biestável tipo JK Mestre-Escarvo contido no CI-7476 através da tabela fornecida pelo fabricante.

PR	CLR	CK	J	K	Q	$\overline{Q}$
0	**0**	**X**	**X**	**X**		
0	**1**	**X**	**X**	**X**		
1	**0**	**X**	**X**	**X**		
1	**1**	**↓**	**0**	**0**		
1	**1**	**↓**	**0**	**1**		
1	**1**	**↓**	**1**	**0**		
1	**1**	**↓**	**1**	**1**		



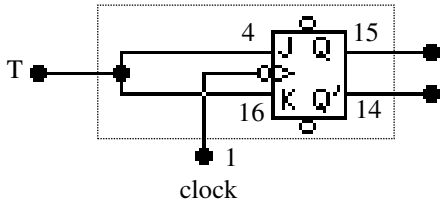
d) A partir do biestável JK, implemente um biestável tipo D e preencha a tabela verdade.

CK	D	Q	$\overline{Q}$
↓	**0**		
↓	**1**		



e) A partir do biestável JK, implemente um biestável tipo T e preencha a tabela verdade. Utilize como clock a chave n° 1.

CK	T	Q	$\overline{Q}$
↓	**0**		
↓	**1**		



f) Repita o item "e" utilizando a chave n° 9 no sinal de clock. Explique o resultado.

_____
_____
_____
_____
_____

IV. CONCLUSÃO:

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_____
_____
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_____

EXPERIÊNCIA

2

REGISTRADORES

Identificação dos alunos:	**Data:**
1.	**Turma:**
2.	
3.	**Professor:**
4.	
5.	**Conceito:**

I. OBJETIVOS:

- Análise do Registrador 74194.

II. MATERIAL UTILIZADO:

- Placa Didática.
- Fonte CC de 5 V.
- CIs: 74194 (1).

III. PROCEDIMENTO EXPERIMENTAL:

1) Verifique o funcionamento do registrador 74194, executando as funções na tabela verdade e compare os resultados com o diagrama de tempos.

2) Execute as seguintes funções com o Registrador 74194 e mostre o resultado através do diagrama de tempos.

a) Limpe a carga do registrador.
b) Faça a carga paralela do dado de 4 bits: 1011.
c) Desloque 4 bits para a direita introduzindo "0" no bit mais significativo.
d) Faça a carga paralela do dado de 4 bits: 0101.
e) Desloque 4 bits para a esquerda introduzindo "1" no bit menos significativo.

Tabela Verdade:

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Diagrama de tempos:

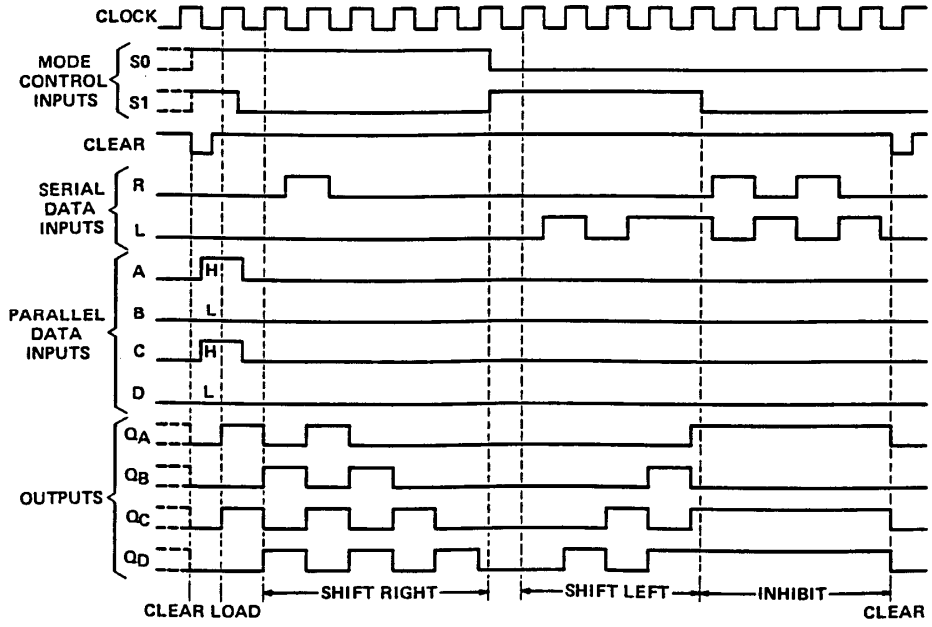
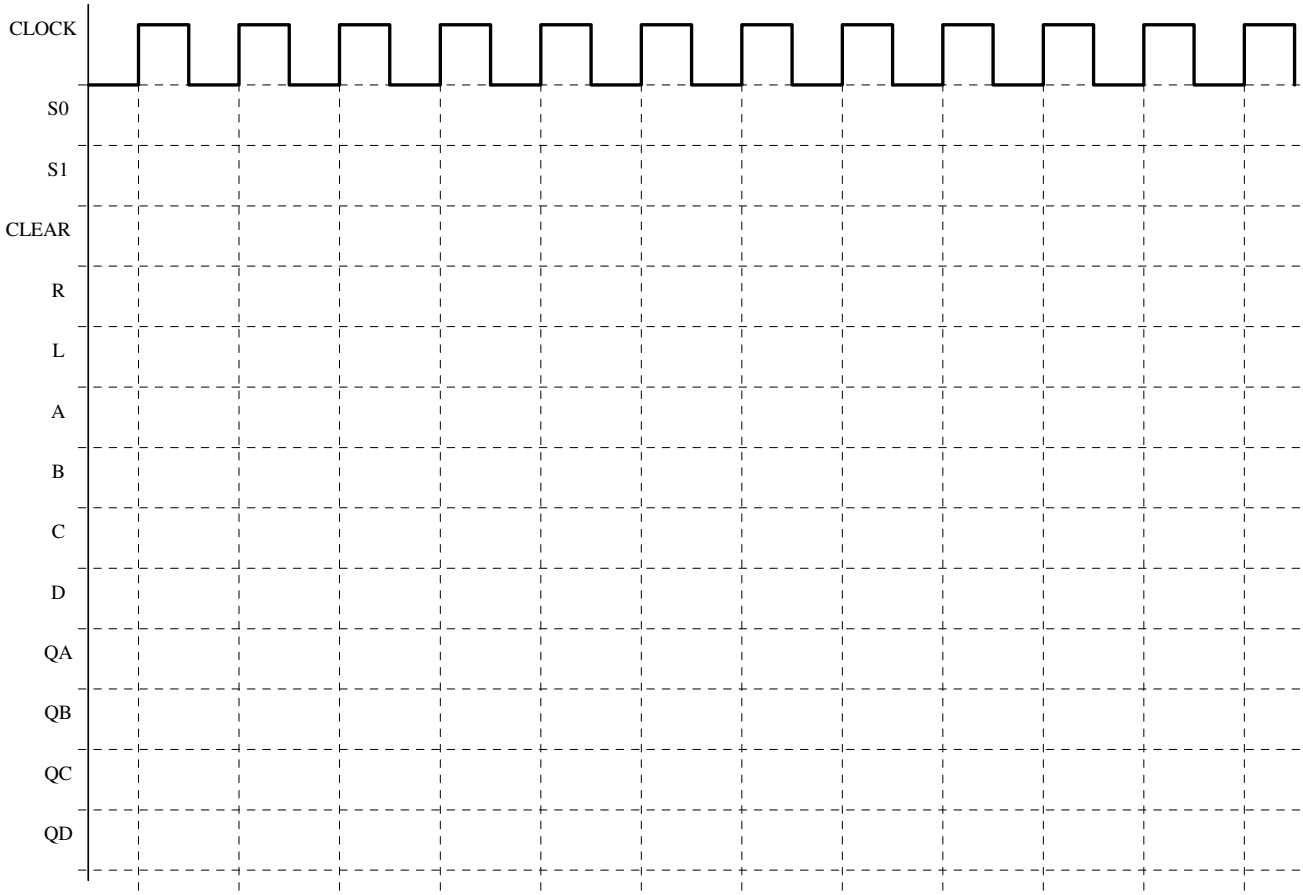


Diagrama de tempos referentes aos itens “b”, “c”, “d” e “e” :



IV. CONCLUSÃO:

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CONTADORES SÍNCRONOS	EXPERIÊNCIA **3**

I. OBJETIVOS:

- Implementação de contadores utilizando biestáveis.

II. MATERIAL UTILIZADO:

- Placa Didática.
- Fonte CC de 5 V.
- CIs: 7476 (1), 7474 (1), 7400 (1), 7402 (1), 7408 (1), 7432 (1).

III. PROCEDIMENTO EXPERIMENTAL:

1) Projetar um contador síncrono de módulo **4,** crescente, utilizando biestáveis tipo **JK** .

2) Projetar um contador síncrono de módulo **3,** decrescente, utilizando biestáveis tipo **D**.

3) Projetar um contador síncrono de módulo ____, _____, utilizando biestáveis tipo ____.

IV. CONCLUSÃO:

_____
_____
_____
_____
_____
_____

CONTADORES ASSÍNCRONOS	EXPERIÊNCIA **4**

Identificação dos alunos:	**Data:**
1.	**Turma:**
2.	
3.	**Professor:**
4.	
5.	**Conceito:**

I. OBJETIVOS:

- Implementação de contadores utilizando o CI 7490.

II. MATERIAL UTILIZADO:

- Placa Didática.
- Fonte CC de 5 V.
- CIs: 7490 (1), 7400 (2).

III. PROCEDIMENTO EXPERIMENTAL:

1) Utilizando o CI 7490, implemente circuitos contadores de módulos 2, 5 e 10 (decimal) e bi-quinário.

a) Módulo 2:

b) Módulo 5:

c) Módulo 10:

d) Bi-quinário:

2) Utilizando o CI 7490, implemente um circuito contador crescente de módulo 7.

IV. CONCLUSÃO:

_____
_____
_____
_____
_____
_____

MEMÓRIA SEMICONDUTORA	EXPERIÊNCIA **5**

Identificação dos alunos:	**Data:**
1.	**Turma:**
2.	
3.	**Professor:**
4.	
5.	**Conceito:**

I. OBJETIVOS:

- Verificar o funcionamento de Memória Semicondutora Integrada.

II. MATERIAL UTILIZADO:

- Placa Didática.
- Fonte CC de 5 V.
- CIs: 74189 (1), 7404 (1).

III. PROCEDIMENTO EXPERIMENTAL:

1) Desenhe e monte um circuito utilizando a memória RAM 74189 de forma que se possa escrever e ler dados em qualquer endereço. Ligue as entrada de endereço no display e a saída de dados nos leds através de um inversor.

Circuito:

2) Dados a serem escritos na memória.

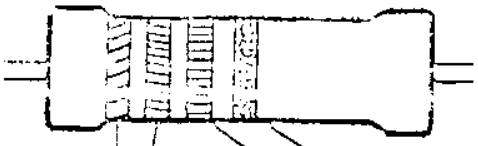
ENDEREÇO	DADO

IV. CONCLUSÃO:

_____
_____
_____
_____
_____

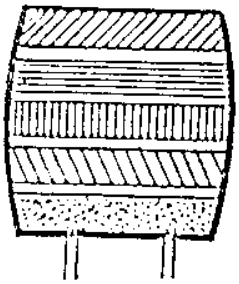
ANEXOS

LEITURA DO VALOR DE RESISTORES



CÓDIGO DO VALOR				CÓDIGO TOLERÂNCIA	
Preto	= 0	Verde	= 5	Marrom	= 1%
Marrom	= 1	Azul	= 6	Vermelho	= 2%
Vermelho	= 2	Violeta	= 7	Dourado	= 5%
Laranja	= 3	Cinza	= 8	Prateado	= 10%
Amarelo	= 4	Branco	= 9	Sem Faixa	= 20%

LEITURA DO VALOR DE CAPACITORES
POLIESTER METALIZADO

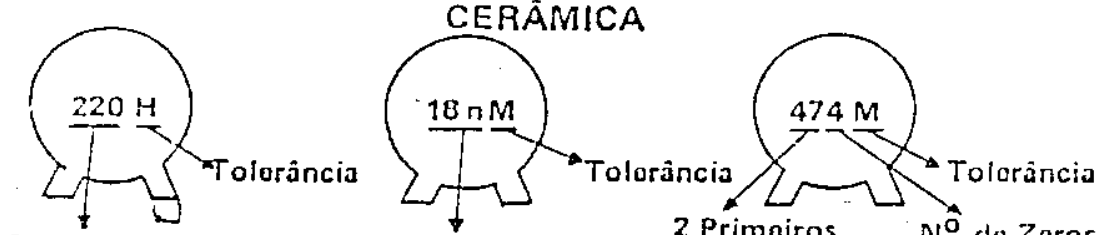


Código de valor igual ao dos resistores

CÓDIGO TOL.	
Preto	= 20%
Branco	= 10%

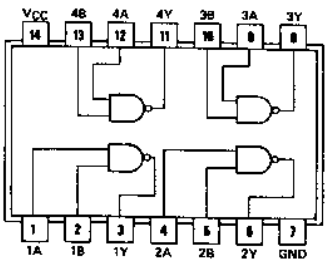
CÓDIGO TENSÃO	
Vermelho	= 250V
Amarelo	= 400V
Azul	= 630V

LEITURA DO VALOR DE CAPACITORES
CERÂMICA

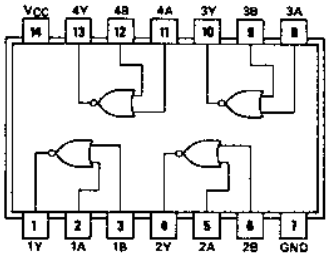


(no caso = 470000 pF - 20%

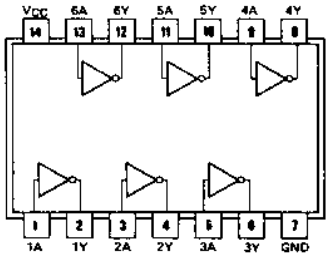
CÓDIGO TOLERÂNCIA		
ATÉ 10 pF	ACIMA DE 10 pF	
B = 0,1 pF	F = 1%	M = 20%
C = 0,25 pF	G = 2%	P = +100% - 0%
D = 0,5 pF	H = 3%	S = +50% - 20%
F = 1 pF	J = 5%	Z = +80% - 20%
G = 2 pF	K = 10%	



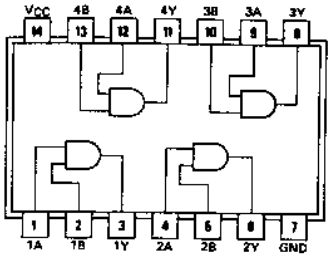
SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)



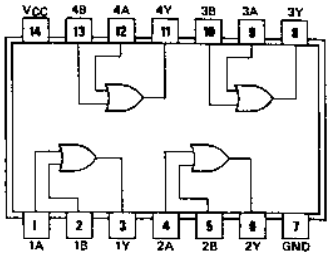
SN5402 (J) SN7402 (J, N)
SN54L02 (J) SN74L02 (J, N)
SN54LS02 (J, W) SN74LS02 (J, N)
SN54S02 (J, W) SN74S02 (J, N)



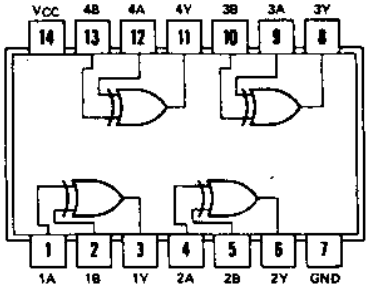
SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)



SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)



SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)



SN5486 (J, W) SN7486 (J, N)
SN54LS86 (J, W) SN74LS86 (J, N)
SN54S86 (J, W) SN74S86 (J, N)

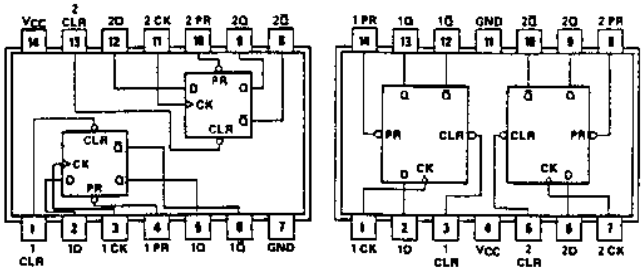
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56



SN5474 (J) SN7474 (J, N) SN5474 (W)
SN54H74 (J) SN74H74 (J, N) SN54H74 (W)
SN54L74 (J) SN74L74 (J, N) SN54L74 (T)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

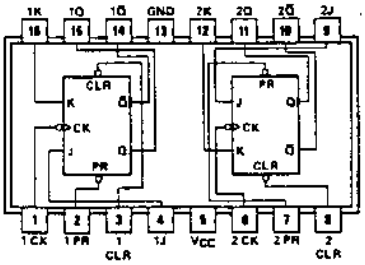
76

'76, 'H76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

'LS76A
FUNCTION TABLE

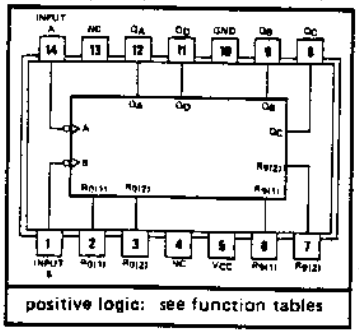
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN5476 (J, W) SN7476 (J, N)
SN54H76 (J, W) SN74H76 (J, N)
SN54LS76A (J, W) SN74LS76A (J, N)

See pages 6-46, 6-50, and 6-56

'90A, 'L90, 'LS90 (TOP VIEW)



positive logic: see function tables

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

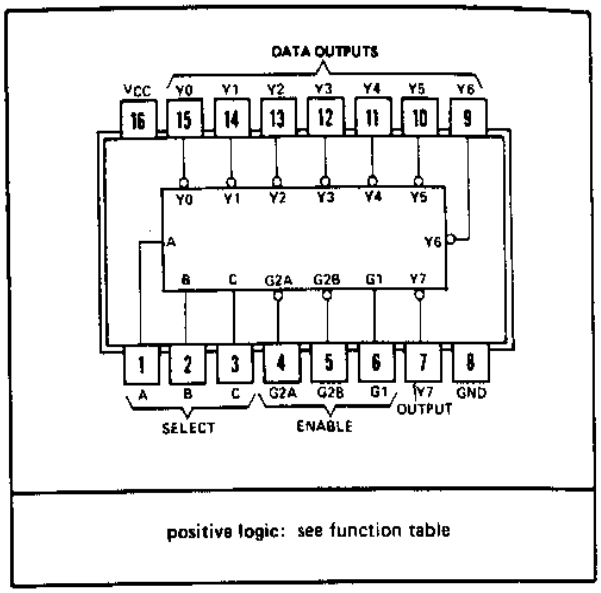
COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)



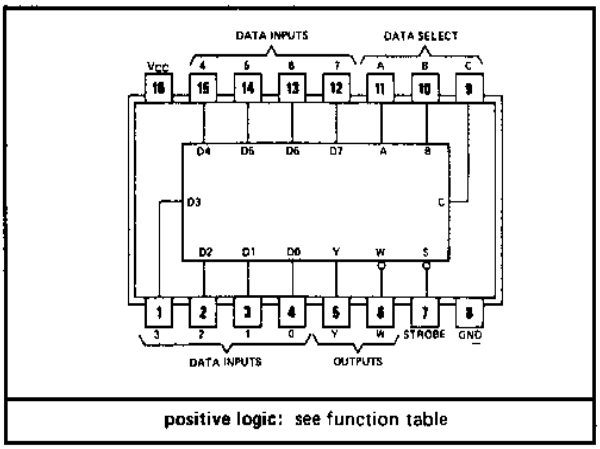
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

SN54151A, SN54LS151, SN54S151 . . . J OR W PACKAGE
SN74151A, SN74LS151, SN74S151 . . . J OR N PACKAGE
(TOP VIEW)



'151A, 'LS151, 'S151
FUNCTION TABLE

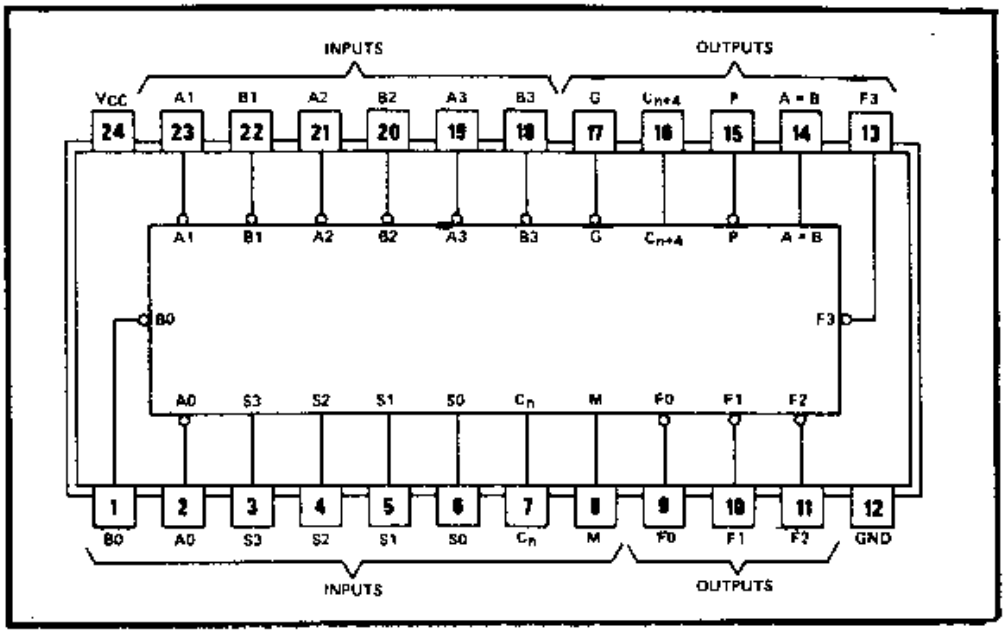
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

D0, D1 . . . D7 = the level of the D respective input

SN54181, SN54LS181, SN54S181 . . . J OR W PACKAGE
SN74181, SN74LS181, SN74S181 . . . J OR N PACKAGE
(TOP VIEW)



SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

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64-BIT RANDOM-ACCESS MEMORIES

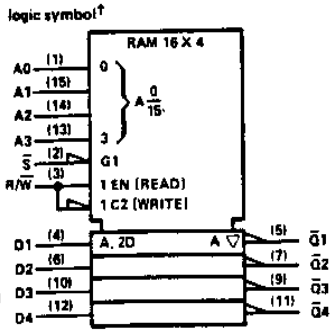
(16 4-bit words; three-state outputs)

typical performance

TYPE	ADDRESS TIME	ENABLE TIME	POWER PER BIT
'LS189A	50 ns	35 ns	2.7 mW
'S189A	25 ns	12 ns	5.9 mW

SN54LS189A (J,FH) SN74LS189A (J,N,FN)
SN54S189A (J,FH) SN74S189A (J,N,FN)

logic symbol†



pin assignments

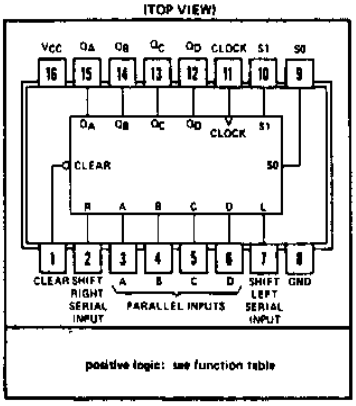
J, N PACKAGES				FH, FN PACKAGES			
1	A0	9	Q̄3	1	nc	11	nc
2	S̄	10	D3	2	A0	12	Q̄3
3	R/W	11	Q̄4	3	S̄	13	D3
4	D1	12	D4	4	R/W	14	Q̄4
5	Q̄1	13	A3	5	D1	15	D4
6	D2	14	A2	6	nc	16	nc
7	Q̄2	15	A1	7	Q̄1	17	A3
8	GND	16	VCC	8	D2	18	A2
				9	Q̄2	19	A1
				10	GND	20	VCC

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level
L = Low Level
X = Don't Care

SN54194, SN54LS194A, SN54S194 . . . J OR W PACKAGE
SN74194, SN74LS194A, SN74S194 . . . J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL							
	S1	S0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.